CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

a plurality of devices connected together and forming circuits;

a switchable current source selectively providing a known current to a PN junction in at least one of said plurality of devices; and

a voltage measurement circuit measuring voltage across said PN junction, measured said voltage corresponding to PN junction temperature.

2. An IC as in claim 1, wherein said switchable current source comprises:

a constant current source; and

a clamping device, selectively shunting current from said constant current source.

3. An IC as in claim 1, wherein said voltage measurement circuit comprises an analog to digital converter.

4. An IC as in claim 1, wherein said voltage measurement circuit comprises a comparator.

5. An IC as in claim 4, wherein a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.

6. An IC as in claim 1, wherein said plurality of devices includes a plurality of field effect transistors (FETs) and said PN junction is a FET body to source/drain junction.

7. An IC as in claim 6, wherein said IC is on a silicon on insulator chip and said plurality of FETs comprises a plurality of P-type FETs (PFETs) and a plurality of N-type FETs (NFETs) connected together in CMOS circuits.

8. An IC as in claim 7, wherein said switchable current source comprises:
a constant current source; and
a clamping FET, selectively shunting current from said constant current source.

9. An IC as in claim 8, wherein said voltage measurement circuit comprises an analog to digital converter.

10. An IC as in claim 8, wherein said voltage measurement circuit comprises a comparator.

11. An IC as in claim 10, wherein a reference voltage is provided to said comparator for comparison against said voltage across said PN junction.

12. A device temperature measurement circuit comprising:
a PN junction in a device;
a constant current source selectively providing current to said PN junction; and
a clamping device, selectively shunting current from said constant current source, a voltage developing across said clamping device and said constant current source, said voltage indicating junction temperature of said PN junction.

13. A device temperature measurement circuit as in claim 12, wherein said clamping device is a field effect transistor (FET) and said PN junction is a FET body to source/drain junction.

14. A device temperature measurement circuit as in claim 13, wherein said FET body is P-type silicon body layer in a NFET and said NFET is in a CMOS inverter.

15. A device temperature measurement circuit as in claim 14, wherein said CMOS inverter is an inverter in a ring oscillator.

16. A device temperature measurement circuit as in claim 15, wherein said ring oscillator comprises a NAND gate connected in series with a plurality of inverters, said inverter being one of said plurality of inverters, an output of said NAND gate being in phase with an output of said inverter.

17. A device temperature measurement circuit as in claim 16, wherein said clamping FET is a NFET and an input of said NAND gate is connected to the gate of said clamping NFET, whereby a gating signal to said input selectively turns said clamping NFET off and blocks oscillation of said ring oscillator.

18. A device temperature measurement circuit as in claim 17, wherein said voltage is provided to a comparator, said comparator comparing said voltage against a reference voltage.

19. A device temperature measurement circuit as in claim 17, wherein said device temperature measurement circuit is on a silicon on insulator (SOI) chip.

20. A method of modeling a field effect transistor (FET) in a circuit on an integrated circuit (IC) chip, said FET being modeled for varying temperature, said method comprising the steps of:

a) determining a voltage to temperature relationship for a PN junction at a known current, said PN junction being a body to source/drain junction of a FET;

b) operating said FET normally; and

c) measuring voltage across said PN junction, measured said voltage indicating the instantaneous temperature of said PN junction, a device temperature model being derived from indicated said instantaneous temperature.

21. A method of modeling said FET as in claim 20, wherein the step (a) of determining said voltage to temperature relationship for the PN junction comprises the steps of:

i) ramping temperature on said PN junction;

ii) providing said known current to said PN junction from an on-chip current source; and

iii) measuring voltage across said PN junction until a maximum selected temperature is reached.

22. A method of modeling said FET as in claim 21, wherein said voltage is periodically measured in step (iii).

23. A method of modeling said FET as in claim 20, wherein the step (b) of operating the FET normally comprises reducing current provided from an on-chip current source to said PN junction.

24. A method of modeling said FET as in claim 23, wherein said on-chip current source is a constant current source and reducing current comprises shunting said constant current source, whereby voltage across said PN junction is below a turn on point for said PN junction.

25. A method of modeling said FET as in claim 20, wherein the measuring step (c) comprises halting operation of said FET.

26. A method of modeling said FET as in claim 25, wherein said FET is included in an inverter in a ring oscillator including said inverter and, halting operation of said FET comprises stopping oscillation of said ring oscillator.

27. A method of modeling said FET as in claim 26, wherein stopping said ring oscillator further comprises turning off a shunt shunting current from an on chip current source, said current flowing through said PN junction.

28. A method of modeling said FET as in claim 27, wherein the measuring step (c) further comprises periodically measuring said voltage across said PN junction.

29. A method of operating an integrated circuit (IC) comprising the steps of:

a) operating a circuit normally,

b) stopping operation of said circuit;

c) checking temperature of at least one PN junction of a device in said circuit; and

d) selectively resuming normal circuit operation.

30. A method of operating an integrated circuit (IC) as in claim 29, wherein whenever in step (c) said temperature is above a threshold temperature, step (d) further comprises initiating an alarm indicating an over temperature.

31. A method of operating an integrated circuit (IC) as in claim 29, further comprising

e) returning to step (b) at the end of a selected operating period.